UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,781	07/25/2001	Jean Louis Calvignac	RAL920010025US1	5146

26675 7590 07/10/2006

DRIGGS, HOGG & FRY CO. L.P.A.
38500 CHARDON ROAD
DEPT. IRA
WILLOUGBY HILLS, OH 44094

EXAMINER	
MAIS, MARK A	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 07/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,781	CALVIGNAC ET AL.	
	Examiner	Art Unit	
	Mark A. Mais	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8,10-13,15-18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-8, 10-13, 15-18, and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-8, 10-13, 15-18, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brewer et al. in view of Dockser (USP 5,860,119).

3. With regard to claims 1, 6, 11 and 16, Brewer et al. discloses a system, multiprocessing system, and method for transmitting multiple data frames to deep packet processing functions in a given sequence, performing the deep packet processing on the frames and forwarding the processed frames to their destination in the same given sequence, comprising:

a) an input buffer for receiving frames for processing, *and having a buffer capacity at least twice the size of the largest frames to be processed* **[Fig. 1, input queues 102 and 103, col. 3, lines 31-37]**;

b) a *Frame Processing Unit* for determining the deep packet processing operation to be performed on each frame **[Packet Forwarding Engines 13 inspect the packet headers and**

performs a filtering function on the packets by destination, whether local or external, col. 3, lines 38-47];

c) an arbitrator for assigning each frame to one of a plurality of processing core engines **[Fig. 1, ASIC 11 determines exit path selection for all packets that enter processing block 101 (what Packet Forwarding Engine 13 to send to) and inserts a sequence number on each packet, col. 3, lines 24-29]**;

d) an output buffer for collecting the processed frames *having a buffer capacity at least twice the size of the largest packet* **[Fig. 1, reorder queues 105, 106, and 107 combine the payload with the header information, col. 6, lines 1-4]**, and

e) a sequencer for forwarding processed frames from the output buffer to their destination in the same order as the frames are received by the input buffer **[Fig. 1, packet ordering block 108 examines reorder queues 105, 106, and 107 for sequence numbers and sends the packets out in the original order, col. 6, lines 1-20]**.

Brewer et al. does not specifically disclose that the unit for determining operation comprises a *Frame Header Processing Unit having a buffer capacity at least twice the size of the largest frame to be processed.* However, Dockser discloses a packet FIFO that makes more effective use of a packet-data channel **[col. 1, lines 8-10]**. Greater-than-one-maximum-sized-packet capacity buffers reduce packet latencies **[col. 2, lines 39-58]**. Dockser discloses FIFOs, which are at least twice the maximum-sized frame length **[col. 3, lines 38-43; col. 4, lines 6-17]**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the input queues of Brewer et al. to have a capacity of at least twice the largest frame

received because such a double/triple/quadruple-sized buffer increases speed and efficiency **[col. 3, lines 5-7]** and makes better use of a packet-data channel **[col.3, lines 40-43]**.

4. With regard to claim 21, Brewer et al. discloses a system for transmitting multiple data frames to deep packet processing functions in a given sequence, performing the deep packet processing on the frames, and forwarding the processed frames to their destination in the same given sequence, comprising

a) an input buffer for receiving frames for processing, having a buffer capacity of at least twice the size of the largest frame size , said buffer incorporated into a Data Moving Unit **[Packet Forwarding Engines 13 inspect the packet headers and performs a filtering function on the packets by destination, whether local or external, col. 3, lines 38-47; Packet Forwarding Engine 13 handles either 2 less-than-200 byte inputs from queues 102 or 1 greater-than-200 byte input from queue 103, col. 4, lines 14-18, and col. 4, line 45 to col. 5, line 14]**;

b) a Frame Header Processing Unit for determining the type of *deep packet* processing operation to be performed on each frame **[Packet Forwarding Engines 13 inspect the packet headers and performs a filtering function on the packets by destination, whether local or external, col. 3, lines 38-47]**;

c) a plurality of processing core engines wherein each core engine has an associated memory for storing a frame assigned to the engine until the engine is free to perform a deep packet processing operation on the frame **[Packet Forwarding Engines 13 inspect the packet**

headers and performs a filtering function on the packets by destination, whether local or external, col. 3, lines 38-47];

d) an arbitrator for assigning an ascending frame sequence number to each frame and for forwarding each frame to one of the core engines for deep-packet processing **[Fig. 1, ASIC 11 determines exit path selection for all packets that enter processing block 101 (what Packet Forwarding Engine 13 to send to) and inserts a sequence number on each packet, col. 3, lines 24-29]**;

e) an output buffer for collecting each frame as it is processed by a core engine, said buffer *having a buffer capacity of at least twice the size of the largest frame size* comprising a portion of the Data Moving Unit **[Fig. 1, reorder queues 105, 106, and 107 combine the payload with the header information, col. 6, lines 1-4]**; and

f) a sequencer for forwarding processed frames from the output buffer to their destination in the same order as they are received by the input buffer **[Fig. 1, packet ordering block 108 examines reorder queues 105, 106, and 107 for sequence numbers and sends the packets out in the original order, col. 6, lines 1-20]**.

Brewer et al. does not specifically disclose input and output buffers *having a buffer capacity at least twice the size of the largest frame to be processed.* However, Dockser discloses a packet FIFO that makes more effective use of a packet-data channel **[col. 1, lines 8-10]**. Greater-than-one-maximum-sized-packet capacity buffers reduce packet latencies **[col. 2, lines 39-58]**. Dockser discloses FIFOs, which are at least twice the maximum-sized frame length **[col. 3, lines 38-43; col. 4, lines 6-17]**. Thus, it would have been obvious to one of ordinary skill in the art at

the time of the invention to have modified the input queues of Brewer et al. to have a capacity of at least twice the largest frame received because such a double/triple/quadruple-sized buffer increases speed and efficiency **[col. 3, lines 5-7]** and makes better use of a packet-data channel **[col.3, lines 40-43]**.

5. With regard to claim 22, Brewer et al. discloses a method of transmitting multiple data frames to deep packet processing functions in a given sequence, performing the deep packet processing on the frames and forwarding the processed frames to their destination in the same given sequence, comprising the steps of:

a) receiving frames into an input buffer that is incorporated into a Data Moving Unit, said buffer having a buffer capacity of at least twice the size of the largest frame size to be processed **[Packet Forwarding Engines 13 inspect the packet headers and performs a filtering function on the packets by destination, whether local or external, col. 3, lines 38-47; Packet Forwarding Engine 13 handles either 2 less-than-200 byte inputs from queues 102 or 1 greater-than-200 byte input from queue 103, col. 4, lines 14-18, and col. 4, line 45 to col. 5, line 14]**;

b) determining the type of deep packet processing operation to be performed on each frame, using a Frame Header Processing Unit **[Packet Forwarding Engines 13 inspect the packet headers and performs a filtering function on the packets by destination, whether local or external, col. 3, lines 38-47]**;

c) assigning each frame to one of a plurality of processing core engines, each frame being stored in a memory associated with a core engine until the engine is free to perform the

processing operation on the frame **[Fig. 1, ASIC 11 determines exit path selection for all packets that enter processing block 101 (what Packet Forwarding Engine 13 to send to) and inserts a sequence number on each packet, col. 3, lines 24-29]**;

d) performing at least one deep-packet processing operation on each frame **[Packet Forwarding Engines 13 inspect the packet headers and performs a filtering function on the packets by destination, whether local or external, col. 3, lines 38-47]**;

e) collecting the processed frames in an output buffer that is incorporated into a Data Moving Unit, *said buffer having a buffer capacity of at least twice the size of the largest frame size to be processed* **[Fig. 1, reorder queues 105, 106, and 107 combine the payload with the header information, col. 6, lines 1-4]**; and

f) sequencing and forwarding processed frames to their destination in the same order as received into the input buffer **[Fig. 1, packet ordering block 108 examines reorder queues 105, 106, and 107 for sequence numbers and sends the packets out in the original order, col. 6, lines 1-20]**.

Brewer et al. does not specifically disclose that input and output buffers *having a buffer capacity at least twice the size of the largest frame to be processed.* However, Dockser discloses a packet FIFO that makes more effective use of a packet-data channel **[col. 1, lines 8-10]**. Greater-than-one-maximum-sized-packet capacity buffers reduce packet latencies **[col. 2, lines 39-58]**. Dockser discloses FIFOs, which are at least twice the maximum-sized frame length **[col. 3, lines 38-43; col. 4, lines 6-17]**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the input queues of Brewer et al. to have a capacity of

at least twice the largest frame received because such a double/triple/quadruple-sized buffer increases speed and efficiency **[col. 3, lines 5-7]** and makes better use of a packet-data channel **[col.3, lines 40-43]**.

6. With regard to claims 2, 7, 12 and 17, Brewer et al. discloses that the input buffer is contained in a Data Moving Unit **[Fig. 1, router system 10, col. 3, lines 20-22]**.

7. With regard to claims 3, 8, 13 and 18, Brewer et al. discloses that the output buffer is also contained in said Data Moving Unit **[Fig. 1, router system 10, col. 3, lines 20-22]**.

8. With regard to claims 5, 10, 15 and 20, Brewer et al. discloses that each core engine has an associated memory for storing a frame assigned to the engine until the engine is free to perform the operation on the frame **[each Packet Forwarding Engine 13 inherently has it's own memory buffer on accepting different-sized and different-rate packets from either of queues 102 or 103 and before performing the filtering function]**.

Response to Arguments

9. Applicant's arguments filed June 23, 2006 have been fully considered but they are not persuasive.

10. Applicants argue that the independent claims (1, 6, 11, 16, 21, and 22), currently amended, recite "deep packet" processing, which Applicants argue is different than processing disclosed in Brewer et al. (described as merely "processing" and/or limited to header inspection) **[Applicant's Amendment dated June 23, 2006, page 9, lines 12-13, page 10, lines 4-7]**. Examiner respectfully disagrees.

11. With respect to independent claims 1, 6, 11, 16, 21 and 22, Brewer et al. discloses that the Packet Forwarding Engines 13-0 through 13-3 perform filtering functions that are performed after inspection of the packet header **[paragraphs 3, 8, and 9 above]**. Thus, after Packet Forwarding Engines 13-0 through 13-3 inspect the packet headers, *they can also determine* if the packet is intended as a local destination within the router and, accordingly, send the packet to the central processor for further processing (thus, a filtering function) **[col. 3, lines 38-47]**. Specifically, the filtering function is interpreted by the examiner as a deep packet process. This deep packet process—a filtering function—is *also* disclosed in Applicant's specification *as a deep packet process* **["...deep-packet processing functions, such as...filtering...[are performed]", (page 1, lines 15-16), "...after processing the frame header and determining what operation needs to be performed...[i.e., filtering]", (page 5, lines 2-4)]**.

12. Applicants argue that the independent claims (1, 6, 11, 16, 21, and 22), currently amended, also maintains packet sequence, which Applicants argue is different than the packet sequence disclosed in Brewer et al. **[Applicant's Amendment dated June 23, 2006, page 9, lines 15-17, page 10, lines 7-8 and lines 16-20]**. Applicants argue that while Brewer et al. deals with exception packets, the invention makes no allowances for exception packets and, therefore, all incoming data frames entering the reception buffer must be maintained in a strict order **[Applicant's Amendment dated June 23, 2006, page 10, lines 17-20]**.

13. With respect to applicant's claim of *not* using exception packets [or using a strict ordering], Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

14. Alternatively, in response to applicant's argument that the reference fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., *not* using exception packets [or using a strict ordering]) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

15. Applicants argue that such a claim limitation of *not* using exception packets is recited in the preambles of the independent claims 1, 6, 16, 21, and 22 **[Applicant's Amendment dated June 23, 2006, page 10, lines 20-22]**.

16. In response to applicant's arguments for claims 1, 6, 16, 21,and 22, the alleged recitation of not using exception packets (strict ordering) has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

17. Applicants further argue that, "although applicants' claims do not specifically refer to the exception packets noted by Brewer et al., the claims [independent claims 1, 6, 11, 16, 21, and 22] nevertheless are clear that they do not accommodate exception packets while maintaining a strict sequence of processing and forwarding packets. [i.e., interpreted as *not* using exception packets]" **[Applicant's Amendment dated June 23, 2006, page 10, line 22 to page 11, line 2]**. Examiner respectfully disagrees.

18. With respect to independent claims 1, 6, 11, 16, 21, and 22, the examiner does not interpret the claimed "given sequence" as affirmatively *not* using exception packets. Having the potential to use an exception packet does not mean that an exception packet has been (or will be) generated (and, therefore, that the sequence *must be* different). The examiner has not interpreted Brewer et al. as from being precluded from maintaining the same sequence that is first input into the input buffer as is output from the output buffer.

19. Applicants argue that Dockser et al. uses only a single FIFO and that, apparently, the use of this FIFO would be inconsistent with the input and output buffers of Brewer et al. **[Applicant's Amendment dated June 23, 206, page 12, lines 17-18]**. Examiner respectfully disagrees.

20. The deficiency of Brewer et al., respectfully restated, is:

> Brewer et al. does not specifically disclose input and output buffers *having a buffer capacity at least twice the size of the largest frame to be processed.*

21. Brewer et al.'s deficiency is in the buffer size. Accordingly:

> Dockser discloses a packet FIFO that makes more effective use of a packet-data channel **[col. 1, lines 8-10]**. Greater-than-one-maximum-sized-packet capacity buffers reduce packet latencies **[col. 2, lines 39-58]**. Dockser discloses FIFOs, which are at least twice the maximum-sized frame length **[col. 3, lines 38-43; col. 4, lines 6-17]**. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the input queues of Brewer

et al. to have a capacity of at least twice the largest frame received because such a double/triple/quadruple-sized buffer increases speed and efficiency **[col. 3, lines 5-7]** and makes better use of a packet-data channel **[col.3, lines 40-43]**.

22. Therefore, the examiner has concluded that the use of a double/triple/quadruple-sized FIFO (disclosed in Dockser) is not inconsistent with the input and output buffers of Brewer et al. (as alleged by applicants).

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Mais whose telephone number is 572-272-3138. The examiner can normally be reached on M-Th 5am-4pm.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MAM
MAM
June 26, 2006

Seema S. Rao 7/6/06
SEEMA S. RAO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600